METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

5   1. Field of the invention

The present invention relates to a method of manufacturing a MOSFET which is formed in a silicon on insulator (SOI) substrate, and more particularly to a method of implanting ions into a silicon layer of the SOI substrate to control a threshold voltage of the SOI-MOSFET. And, the present invention relates to a semiconductor device

10   which is formed in the SOI substrate, and more particularly to a peak ion concentration of the silicon layer of the SOI-MOSFET.

The present application claims priority under 35 U.S.C. §1 19 to Japanes Patent Application No. 2001-68895, filed March 12, 2001, which is herein incorporated by reference in its entirely for all purposes.

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2. Description of the related art

A conventional method of manufacturing a semiconductor device will be described below with reference to the cross-sectional views of Figs. 19(a) through 19(f) and Figs. 20(a) through 20(c).

20   At first, an SOI substrate 501 is prepared having a silicon substrate 500, an oxid film 502 and an SOI layer 504, as shown in Fig. 19(a).   A pad oxide film 506 is formed on th SOI layer 504, as shown in Fig. 19(b), and th n a nitride film (Si_3N_4) 508

is formed on the pad oxide film 506, as shown in Fig. 19(c).

Then, an isolation film 503 is formed by a local oxidation (LOCOS) method or a shallow trench isolation (STI) method, as shown in Fig. 19(d). Thereafter, the pad oxide film 506 is removed, as shown in Fig. 19(e), and then a thin oxide film 510 is

5   formed on the SOI layer 504, as shown in Fig. 19(f). A thickness of the thin oxide film 510 may be less than 10 nm.

Then, impurity ions 512 are implanted into the SOI layer 504, as shown in Fig. 20(a). In the n-type SOI-MOSFET, a p-type impurity ion is implanted, and in the p-type SOI-MOSFET, an n-type impurity ion is implanted. Then, a gate electrode 514 is

10   formed on the thin oxide film, as shown in Fig. 20(b). The gate electrode 514 is composed of a poly-silicon, for example. Finally, lightly doped drain (LDD) regions which includes source and drain regions 516 are formed with the use of side walls 518, as shown in Fig. 20(c).

Fig. 21 is a graph for illustrating the relationship between a gate length and a

15   threshold voltage of the conventional SOI-MOSFET. As the gate length of the SOI-MOSFET is reduced from 0.5 μm, the threshold voltage of the device gradually falls. However, as the gate length is reduced even further, the fall in the threshold voltage becomes more pronounced, until eventually small reductions in gate length result in large drops in the threshold voltage. This is known as a "short channel effect". As

20   such when the gate length of the SOI-MOSFET is designed to be about 0.35 μm, the thr shold voltage does not vary to any great xtent as a result of manufacturing variation in the gate length. Howev r, when the gat length is designed to be less

2

than 0.15 μm, the threshold voltage can exhibit wid   variation even with only small variation in the manufactured gate length.

Fig. 22 is a graph for illustrating the relationship between a gate length and a sub-threshold coefficient of the conventional SOI-MOSFET.   As the gate length of the

5   SOI-MOSFET is reduced from 0.5 μm, the sub-threshold coefficient S (mV/dec.) gradually rises.   However, as the gate length is reduced even further, the rise in the sub-threshold coefficient S becomes more pronounced, until eventually small reductions in gate length result in large increases in the sub-threshold coefficient S. Also, the larger the sub-threshold coefficient S, the larger becomes an off-leak current.

10   As such, small reductions in gate length can result in large increases in the sub-threshold coefficient S and in the off-leak current.

Figs. 23(a) and 23(b) are graphs for illustrating relationships between a thickness of the SOI layer and a threshold voltage of the conventional SOI-MOSFET when the SOI-MOSFET has two kinds of gate length.   It is known a relatively thin SOI

15   layer to help mitigate the short channel effect.   However, if the SOI layer is too thin, the threshold voltage suddenly falls off, as shown in Figs. 23(a) and 23(b).

The conventional SOI-MOSFET is disclosed in an article of Proceeding 1995 IEEE International SOI Conference, Oct. 1995, pp.116-117, "Characteristics of Submicrometer LOCOS Isolation", published on October, 1995.

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SUMMARY OF THE INVENTION

It is an objective of the invention to provide a method of manufacturing a

3

semiconductor device and a semiconductor device so as to effectiv ly inhibit the short channel effect resulting from a reduction of the gate length attendant with miniaturization of the SOI-MOSFET.

To achieve this object, in a method of manufacturing a semiconductor device and a semiconductor device, impurity ions are implanted into the SOI layer so that a distribution of an impurity ion concentration in the SOI layer inhibits a reduction in a threshold voltage (Vth-rolloff) of the device.

According to the present invention, a reduction in a potential barrier can be effectively inhibited, which in turn can effectively inhibit the short channel effect resulting from a reduction in the gate length.

The above and further objects and novel features of the invention will more fully appear from the following detailed description, appended claims and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Figs. 1(a) through 1(f) and Figs. 2(a) through 2(c) are cross-sectional views for xplaining a method of manufacturing a semiconductor device according to a first

4

preferred embodiment of the present invention;

Fig. 3 is a diagram showing a distribution of an ion concentration according to the first preferred embodiment;

Figs. 4 is a diagram showing three distributions of the ion concentration in which the peak ion concentrations are different from one another;

Fig. 5 is a diagram showing the relationship between a gate length and a threshold voltage of an SOI-MOSFET, for each of the three distributions of the ion concentration shown in Fig. 4;

Figs. 6(a) and 6(b) show the results of a simulation depicting the relationship between the peak ion concentration and a reduction in the threshold voltage;

Figs. 7(a) and 7(b) are diagrams showing potential distributions of the SOI-MOSFET;

Figs. 8(a) and 8(b) are cross-sectional views for explaining a method of manufacturing a semiconductor device according to a second preferred embodiment of the present invention;

Fig. 9 is a diagram for explaining a distribution of an ion concentration according to the second preferred embodiment.

Fig. 10 is a cross-sectional view for explaining a pocket ion-implantation;

Fig. 11 is a diagram showing distributions of the ion concentration when th pocket ion-implantation is performed to achieve the pockets as shown in Fig. 10, and when such pocket ion-implantation is not performed (i.e., the pockets as shown in Fig. 10 are not formed), respectively;

Fig. 12 is a diagram showing relationships between a gate length and a threshold voltage when the ion-implantation is performed by the pocket ion-implantation and is not performed by the same, respectively;

Figs. 13(a) through 13(d) are cross-sectional views for explaining a method of manufacturing a semiconductor device according to a third preferred embodiment of the present invention;

Fig. 14 is a diagram showing distributions of an ion concentration when a heat treatment is performed and is not performed, respectively;

Fig. 15 is a diagram showing relationships between a gate length and a threshold voltage when the heat treatment is performed and is not performed, respectively;

Figs. 16(a) through 16(c) are cross-sectional views for explaining a method of manufacturing a semiconductor device according to a fourth preferred embodiment of the present invention;

Fig. 17 is a diagram for showing a distribution of an ion concentration according to the third preferred embodiment;

Figs. 18(a) and 18(b) are diagrams showing a sub-threshold coefficient S and a dispersion of the same for each of four concentration distributions having different peak ion concentrations;

Figs. 19(a) through 19(f) and Figs. 20(a) through 20(c) are cross-sectional views for explaining a conventional method of manufacturing a semiconductor device;

Fig. 21 is a diagram showing a relationship b tween a gate length and a

6

threshold voltage of a conventional SOI-MOSFET;

Fig. 22 is a diagram showing a relationship between a gate length and a sub-threshold coefficient of the conventional SOI-MOSFET; and

Figs. 23(a) and 23(b) are diagrams showing relationships between a thickness of an SOI layer and a threshold voltage of the conventional SOI-MOSFET which has different gate lengths.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will hereinafter be described in detail with reference to the accompanying drawings. The drawings used for this description typically illustrate major characteristic parts in order that the present invention will be easily understood.

Figs. 1(a) through 1(f) and Figs. 2(a) through 2(c) are cross-sectional views for explaining a method of manufacturing a semiconductor device according to a first preferred embodiment of the present invention. An SOI substrate 101 is first prepared which includes a silicon substrate 100, an oxide film 102 and an SOI layer 104, as shown in Fig. 1(a). A pad oxide film 106 is formed on the SOI layer 104, as shown in Fig. 1(b), and then a nitride film (Si_3N_4) 108 is formed on the pad oxide film 106, as shown in Fig. 1(c). Then, an isolation film 103 is formed by a LOCOS method or an STI method, as shown in Fig. 1(d). Thereafter, the pad oxide film 106 is removed, as shown in Fig. 1(e), and then a thin oxide film 110 is formed on the SOI layer 104, as shown in Fig. 1(f). A thickness of the thin oxide film 10 may be less

than 10 nm.

Then, as shown in Fig. 2(a), impurity ions 112 are implanted into the SOI layer 104.

Fig. 3 is a diagram showing a distribution of an ion concentration of the impurity ions 112 implanted into the SOI layer 104. A p-type impurity ion is implanted when the SOI-MOSFET is an n-type device. An n-type impurity ion is implanted when th SOI-MOSFET is a p-type device. The threshold voltage of the SOI-MOSFET is controlled by characteristics of the ion-implantation. That is, the first preferred embodiment is characterized by the distribution of the ion concentration of the impurity ions 112 implanted into the SOI layer 104. Particularly, the distribution of the ion concentration is set such that a peak ion concentration is located at or between an intermediate horizontal plane 109 (1/2 Tsoi) and a bottom surface 111 (Tsoi) of the SOI layer 104, where Tsoi is a depth of the SOI layer 104. The intermediate horizontal plane 109 (1/2 Tsoi) is a horizontal plane extending halfway between top and bottom surfaces 107, 111 of the SOI layer 104. The distribution of the ion concentration is set such that the peak ion concentration is located at or between the intermediate horizontal plane 109 (1/2 Tsoi) and the bottom surface 111 (Tsoi) of the SOI layer 104.

Then, a gate electrode 114 is formed on the thin oxide film 106, as shown in Fig. 2 (b). The gate electrode 114 is composed of a poly-silicon, for example. Finally, lightly doped drain (LDD) regions which include source and drain regions 116 ar formed with the us of side walls 118, as shown in Fig. 2(c).

Fig. 4 is a diagram showing three distributions of the ion concentration in which the peak ion concentrations are different from one another. A curve A (Process A) shows the case where the peak ion concentration is located near the top surface 107 of the SOI layer 104. A curve B (Process B) shows the case where the peak ion concentration is located between the intermediate horizontal plane 109 (1/2 Tsoi) and the bottom surface 111 (Tsoi) of the SOI layer 104. A curve C (Process C) shows the case where the peak ion concentration is located below the bottom surface 111 (Tsoi) of the SOI layer 104.

Fig. 5 is a diagram showing a relationship between a gate length and a threshold voltage Vth of an SOI-MOSFET, for each of the three distributions of ion concentration shown in Fig. 4. Similarly the conventional SOI-MOSFET, each of curves A, B and C shows that as the gate length of the SOI-MOSFET is shortened, the threshold voltage Vth gradually falls. However, the reduction in the threshold voltage Vth (Vth-rolloff) is the smallest for curve B. Where the peak ion concentration is located at or between the intermediate horizontal plane 109 (1/2 Tsoi) and the bottom surface 111 (Tsoi) of the SOI layer 104.

Figs. 6(a) and 6(b) are results of a simulation showing a relationship between the peak ion concentration and the reduction in the threshold voltage Vth (Vth-rolloff). Fig. 6(a) is the results of the simulation of a plurality of different peak ion concentrations into the SOI layer 104, which is 40 nm (0.04 μm) in depth. Each distribution exhibits the same threshold voltage Vth@Lgate=1 μm when a gate length of the SOI-MOSFET is 1 μm (a long channel). Consequ ntly, th simulation of Fig.

6(a) can accurately to compar a short channel effect (the reduction in the threshold voltage Vth (Vth-rolloff)), when the gate length of the SOI-MOSFET is short (a short channel).

The threshold voltage Vth@Lgate=0.15 μm is calculated when the gate length

5 of the SOI-MOSFET is 0.15 μm (a short channel). In this simulation, a difference between the threshold voltage Vth@Lgate=1 μm and the threshold voltage Vth@Lgate=0.15 μm is defined as the reduction in the threshold voltage Vth (Vth-rolloff). Then, the relationship between the reduction in the threshold voltage Vth (Vth-rolloff) and the peak ion concentration depth within the SOI layer 104 is shown in

10 Fig. 6(b). As shown, the reduction in the threshold voltage Vth (Vth-rolloff) is substantial when the peak ion concentration is located at a more shallow depth than the intermediate horizontal plane 109 (1/2 Tsoi) of the SOI layer 104 (0 < 0.5), and is inhibited when the peak ion concentration is located at or below the intermediate horizontal plane 109 (1/2 Tsoi) of the SOI layer 104 (0.5 =< 1).

15 Figs. 7(a) and 7(b) illustrate potential distributions of the SOI-MOSFET. Fig. 7(a) shows the potential distribution of the SOI-MOSFET which is manufactured by the Process A in which the peak ion concentration is located near the top surface 107 of the SOI layer 104. Fig. 7(b) shows the potential distribution of the SOI-MOSFET which is manufactured by the Process B in which the peak ion concentration is located

20 at or between the intermediate horizontal plane 109 (1/2 Tsoi) and the bottom surface 111 (Tsoi) of the SOI layer 104. A gate voltag Vg of th SOI-MOSFET is

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substantially the same as the threshold voltage Vth (Vg ≒ Vth). A drain region of the SOI-MOSFET is connected to a voltage supply.

As shown in Fig. 7(a), a potential barrier of the SOI-MOSFET manufactured by the Process A falls substantially from the drain region side due to a voltage which is

5 impressed by the voltage supply. On the other hand, as shown in Fig. 7(b), the potential barrier of the SOI-MOSFET manufactured by the Process B falls only slightly from the drain region side due to the voltage which is impressed by the voltage supply. Thus, the falling of the potential barrier of the SOI-MOSFET manufactured by the Process B is smaller than that of the Process A. That is, the potential barrier of the

10 SOI-MOSFET falls to a much lesser extend when the peak ion concentration is between the intermediate horizontal plane 109 (1/2Tsoi) and the bottom surface 111 (Tsoi) of the SOI layer 104.

According to the first preferred embodiment of the present invention, since the distribution of the ion concentration is set such that the peak ion concentration is

15 located at or between the intermediate horizontal plane 109 (1/2 Tsoi) and the bottom surface 111 (Tsoi) of the SOI layer 104, the reduction in the potential barrier can be effectively inhibited. Therefore, the method of the first preferred embodiment can effectively inhibit the short channel effect resulting from a reduction in the gate length attendant with miniaturization of the SOI-MOSFET.

20 Figs. 8(a) and 8(b) are cross-sectional views describing a method of manufacturing a semiconductor device according to a second preferred embodiment of th present invention. Fig. 9 is a diagram showing a distribution of an ion

concentration when impurity ions 212 are implanted into an SOI layer 204. Th second preferred embodiment includes the same process steps as shown in Figs. 1(a) through 1(f) of the first preferred embodiment.

After a thin oxide film 210 is formed on the SOI layer 204 (similar to Fig. 1(f)), a

5 gate electrode 214 is formed on the thin oxide film 210. Then, the impurity ions 212 are implanted into the SOI layer 204 by a pocket ion-implantation, as shown in Fig. 8(a). The impurity ions 212 are implanted from an oblique direction which is set at a predetermined angle relative to an SOI substrate 201. Similar to the first preferred embodiment, a distribution of an ion concentration of the impurity ions 212 implanted

10 into the SOI layer 204 is set such that a peak ion concentration is located at or between an intermediate horizontal plane 209 (1/2 Tsoi) and a bottom surface 211 (Tsoi) of the SOI layer 204, as shown in Fig. 9. A p-type impurity ion is implanted when the SOI-MOSFET is an n-type device, and an n-type impurity ion is implanted when the SOI-MOSFET is a p-type device.

15 Fig. 10 is a cross-sectional view for explaining a pocket ion-implantation. As shown in Fig. 10, impurity regions 215 are formed as pockets by the ion-implantation. An ion-implantation angle of the impurity ion 212 is properly changeable in accordance with the various process conditions.

As shown in Fig. 8(b), lightly doped drain (LDD) regions which include source

20 and drain regions 216 are formed with the use of side walls 218.

Fig. 11 is a diagram showing distributions of the ion concentration when the pock t ion-implantation is performed to achiev the pockets as shown in Fig. 10, and

12

when such pocket ion-implantation is not performed (i.e., the pockets as shown in Fig. 10 are not formed), respectively. The distribution of the ion concentration which is below the gate electrode 214 and near a surface between an oxide film 202 and th SOI layer 204, when the ion-implantation is not performed by the pocket ion-implantation, is a dilute and a substantially homogeneous distribution.

At the same time, the distribution of the ion concentration which is below the gate electrode 214 and near the surface between the oxide film 202 and the SOI layer 204, when the ion-implantation is performed by the pocket ion-implantation, shows that the impurity ion concentration increases around both surfaces between the SOI layer 204 under the gate electrode 214 and the source and drain regions 216. Therefore, the second preferred embodiment of the present invention can effectively inhibit the reduction in the potential barrier which runs from the drain region side.

Fig. 12 is a diagram showing a relationship between the gate length and th threshold voltage when the pocket ion-implantation is performed and is not performed, respectively. The reduction in the threshold voltage Vth (Vth-rolloff) is not so substantial even though the gate length is narrowed, when the pocket ion-implantation is performed, as shown in Fig. 12. The manufacturing method of the second preferred embodiment can be effectively inhibited the short channel effect even though the gate length is narrowed as a result of miniaturization of the SOI-MOSFET.

According to the second preferred embodiment of the present invention, since the pocket ion-implantation is performed after forming the gate electrode 214, and the distribution of th ion concentration is set such that the p ak ion concentration is

13

located b tween the intermediate horizontal plane 209 (1/2 Tsoi) and the bottom surface 211 (Tsoi) of the SOI layer 104, the impurity ion concentration can be increased around both surfaces between the SOI layer 104 under the gate electrode 214 and the source and drain region 216. Therefore, the manufacturing method of

5   the second preferred embodiment can effectively inhibit the reduction in the potential barrier which runs from the drain region side. In other words, the short channel effect can be effectively inhibited.

Fig. 13(a) through 13(d) are cross-sectional views for explaining a method of manufacturing a semiconductor device according to a third preferred embodiment of

10   the present invention. The third preferred embodiment includes the same process steps as shown in Fig. 1(a) through 1(f) of the first preferred embodiment.

After a thin oxide film 310 is formed on an SOI layer 304 (similar to Fig. 1(f)), impurity ions 312 are implanted into the SOI layer 304, as shown in Fig. 13(a). A distribution of an ion concentration of the impurity ions 312 implanted into the SOI

15   layer 304 is set such that a peak ion concentration is located between a top surface and an intermediate plane of the SOI layer 304. A p-type impurity ion is implanted when the SOI-MOSFET is an n-type device, and an n-type impurity ion is implanted when the SOI-MOSFET is a p-type device.

Then, a heat treatment is carried out, as shown in Fig. 13(b). The heat

20   treatment may be conducted at a temperature range of 950°C ~ 1000°C, and in an inert (x. Nitrogen gas N_2) atmosph r⁻ or in a vacuum atmosphere. The heat treatment causes the impurity ions 312 to diffuse into a deep region of th SOI layer

14

304.   In detail, the impurity ions 312 are diffused to achi ve a substantially homogeneous ion distribution a described below (Fig. 14).   This heat treatment is called a channel anneal.

Fig. 14 is a diagram showing distributions of the ion concentration when the heat treatment is performed and is not performed, respectively.   Due to a diffusion of the impurity ions 312 by the heat treatment after the ion-implantation, the impurity ion concentration of the SOI layer 304 becomes substantially homogeneous, as shown in Fig. 14.

Fig. 15 is a diagram showing a relationship between the gate length and the threshold voltage when the heat treatment is performed and is not performed after th ion-implantation, respectively.   As shown in Fig. 15, when the heat treatment is performed after the implantation of the impurity ions 312, the reduction in the threshold voltage Vth (Vth-rolloff) is not as substantial as the gate length is reduced.   Th manufacturing method of the third preferred embodiment can effectively inhibit the short channel effect resulting from miniaturization of the SOI-MOSFET.

As shown in Fig. 13(c), a gate electrode is formed on the thin oxide film 310. Then, the lightly doped drain (LDD) regions which include source and drain regions 316 are formed using side walls 318, as shown in Fig. 13(d).

According to the preferred third embodiment of the present invention, since the heat treatment allows for the impurity ion concentration of the deep region of the SOI layer 304 to be increased and the impurity ion concentration of the SOI layer 304 to be mad the substantially homogeneous, the reduction in the potential barrier which runs

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from the drain region side can be effectively inhibited. Therefore, the manufacturing method of the third preferred embodiment can effectively inhibit the short channel effect.

While the third preferred embodiment of the present invention presents an
5 example in which the heat treatment is conducted at the temperature range of 950°C ~ 1000 °C after the ion-implantation, the invention is not limited to this range, and a temperature in excess of 850 °C is usually sufficient to achieve the desired dispersion.

Further, while the third preferred embodiment of the present invention presents an example in which the nitrogen N2 atmosphere is used for the heat treatment, the
10 present invention is not limited to this example and other inert gas atmospheres (ex. Argon Ar and Helium He) may be used.

Fig. 16(a) through 16(c) are cross-sectional views for explaining a method of manufacturing a semiconductor device according to a fourth preferred embodiment of the present invention. The fourth preferred embodiment includes the same process
15 steps as shown in Fig. 1(a) through 1(f) of the first preferred embodiment.

Then, impurity ions 412 are implanted into an SOI layer 404, as shown in Fig.16(a). A p-type impurity ion is implanted when the SOI-MOSFET is an n-typ device, and an n-type impurity ion is implanted when the SOI-MOSFET is a p-type device.

20 The fourth preferred embodiment differs from prior embodiments with respect to the preferred rang of a peak ion concentration.

Fig. 17 is a diagram showing a distribution of an ion concentration wh n

16

impurity ions are implanted into an SOI layer.   Fig. 17 shows top and bottom surfaces 407, 411 of the SOI layer 404, an intermediate horizontal plane 409 (1/2 Tsoi) of the SOI layer 404, and the distribution of the ion concentration.   The distribution of the ion concentration is set such that the peak ion concentration is located within a range

5   of 1/2Tsoi ± 0.1Tsoi, where Tsoi is a depth of the SOI layer 404, when the impurity ions 412 are implanted into the SOI layer 404.

Then, a gate electrode 414 which is composed of a poly-silicon is formed on a thin oxide film 410, as shown in Fig. 16(b).   Finally, lightly doped drain (LDD) regions which include source and drain regions 416 are formed using side walls 418, as

10   shown in Fig. 16(c).

Fig. 18(a) is a diagram showing a relationship between an sub-threshold coefficient S and a dispersion of the same, when the impurity ions are implanted into the SOI layer 404 to achieve four distributions (I, II, III and IV) of the ion concentration having different peak ion concentrations from one another.   Fig. 18(b)

15   is a histogram showing a relationship between the sub-threshold coefficient S and the number of samples of the same, when the impurity ions are implanted into the SOI layer 404 according to four distributions (I, II, III and IV) of the ion concentration.

Referring also to Fig. 17, distribution (I) is the case were the peak ion concentration is located at a lesser depth than the preferred range of 1/2Tsoi - 0.1Tsoi

20   (PEAK ION CENCENTRATION < 1/2Tsoi - 0.1Tsoi).

Distribution (II) is the case were the peak ion concentration is located at 1/2Tsoi - 0.1Tsoi (PEAK ION CENCENTRATION = 1/2Tsoi - 0.1Tsoi.

17

Distribution (III) is the case were the peak ion concentration is locat d at 1/2Tsoi + 0.1Tsoi (PEAK ION CENCENTRATION = 1/2Tsoi + 0.1Tsoi).

Distribution (IV) is the case were the peak ion concentration is located at a greater depth than the preferred range of 1/2Tsoi + 0.1Tsoi (PEAK ION CONCENTRATION > 1/2Tsoi + 0.1Tsoi).

As shown in Fig. 18(a) and 18(b), the sub-threshold coefficients S of distributions (II) and (III) are smaller than those distributions (I) and (IV). Further, the dispersions of the sub-threshold coefficients S of distributions (II) and (III) are smaller than those distributions (I) and (IV).

The SOI-MOSFET which is formed due to an ion implantation of near the top surface 407 of the SOI layer 404 can not inhibited the reduction in the potential barrier which runs from the drain region, as in distribution (I). Therefore, the sub-threshold coefficient S rises since the threshold voltage Vth falls with a reduction in the gate length.

Since a depletion rate of the SOI layer 404 falls when the impurity ions 412 are implanted into the vicinity of bottom surface 411 of the SOI layer 404, the threshold coefficient S rises and the dispersion of the threshold coefficient S increases as in distribution (IV).

According to the fourth preferred embodiment of the present invention, since the distribution of the ion concentration is set such that the peak ion concentration is located within a range of 1/2Tsoi ± 0.1Tsoi, where Tsoi is a depth of the SOI layer 404, a characteristic of the sub-thr shold coefficient S and the dispersion of the sub-

threshold coefficient S can be optimized. Moreover, since the reduction in the potential barrier which runs from the drain region can be effectively inhibited, the method of the fourth preferred embodiment can effectively inhibit the short channel effect caused by reduction the gate length attendant with miniaturization of the SOI-

5   MOSFET.

As described above, the method of manufacturing semiconductor device and the semiconductor device according to the present invention can effectively inhibit the reduction in the potential barrier which runs from the drain region. Therefore, the method and device of the present invention can effectively inhibit the short channel

10   effect resulting from a reduction in the gate length attendant with miniaturization of the SOI-MOSFET.

The present invention has been described with reference to illustrative embodiments, however, this invention must not be considered to be confined only to the embodiments illustrated. Various modifications and changes of these illustrative

15   embodiments and the other embodiments of the present invention will become apparent to those skilled in the art with reference to the description of the present invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.